

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Minsheng Wang

Appl. No.: to be assigned

Filed: February 25, 2004

For: State-Delayed Technique and System to Remove Tones of Dynamic Element Matching Confirmation No.: to be assigned

Art Unit: 2819

Examiner: Peguy Jean Pierre Atty. Docket: 1875.3760001

Information Disclosure Statement

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicant has listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may

not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

- 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.
- 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date 233202-1

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of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application. a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1). b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2). c. Attached is our PTO-2038 Credit Card Payment Form in the amount of \$_____ in payment of the fee under 37 C.F.R. § 1.17(p). 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

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- a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.
- 6. A concise explanation of the relevance of the non-English language document(s) appears below:
- 7. Copies of the documents are submitted herewith.

8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 10/434,220, filed May 9, 2003, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michelle K. Holoubek Patent Agent for Applicant

Registration No. 54,179

Date: <u>February 25, 2004</u>

1100 New York Avenue, N.W. Washington, D.C. 20005-3934 (202) 371-2600

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	AA1		3,742	06-2003	Hossack, David MacDonald				
	AB1	6,29	2,124	09-2001	Hanada et al.				
	AC1	6,12	4,813	09-2000	Robertson et al.				
	AD1	6,51	8,899	02-2003	Yu, Xianggang				
	AE1	6,57	7,261	06-2003	Brooks et al.				
	AF1	6,54	5,623	04-2003	Yu, Paul C.				
	AG1	6,46	6,153	10-2002	Yu, Paul C.				
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			Yasuda e	et al "A Third	-Order Δ-Σ Modulator Using	Second	Order Noise-Si	haning	
			Dynamic	Flement Mate	ching," IEEE Journal of Solid-	State C	ircuite Vol. 22	No 12 no	
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			Kwan <i>et a</i>	al., "A Stereo	Multibit ΣΔ DAC with Asynch	ronous	Master-Clock Ir	nterface,"	
		1			State Circuits, Vol. 31, No. 12				
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	1875.3760001	To be assigned	
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	Adams et al., "A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling," IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, pp. 1871-1878, IEEE AR 2 (December 1998).							Shaped 1-1878, IEEE
	Welz et al., "Simplified Logic for First-Order and Second-Order Mismatch-Shaping Digital-to-Analog Converters," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 48, No. 11, pp. 1014-1027, IEEE, (November 2001).							
	Grilo et al., "A 12-mW ADC Delta-Sigma Modulator With 80 dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver," IEEE Journal of Solid -State Circuits, Vol. 37, No. 3, pp. 271-278, IEEE (March 2002)							
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	AR	3	Ian Galton on Circuits (October 1	s and Systems	aping of Circuit Errors in 3 - II: Analog and Digital S	Digital-to-Analog C lignal Processing Vo	onverters," IEEI d. 44, No. 10 pp.	E Transactions . 808-817, IEEE
	AS 3 Norsworthy et al., Delta-Sigma Data Converters: Theory, Design and Simul IEEE Press.						nd Simulation,	pp. 185-186,
	AT	3		et al., Advance	ed Digital Signal Process 994).	sing: Theory and A	pplications, pp.	357-364,
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	AR	4	Morteza Va Algorithm	adipour, "Tec in Σ-Δ Modu	hniques for Preventing lators," IEEE Transaction g, Vol. 47, No. 11, pp. 1	Tonal Behavior on Circuits an	of Data Weighted nd Systems-II: A	nalog and	
AS 4 Chen et al., "Some Obser the 1998 International Systems of the 1998 I					ervations on Tone Behav ymposium on Circuits a	vior in Data Weig nd Systems, Vol	ghted Averaging, 1, pp. 500-503,	" Proceedings of IEEE (1998).	
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	ATTY. DOCKET NO. 1875.3760001	APPLICATION NO. To be assigned	
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	AR	<u>5</u>	Radke et a	l., "A 14-Bit Cu	rrent-Mode ΣΔ DAC Based e Circuits, Vol. 35, No. 8, pp	Upon Rotat	ed Data Weight	ed Averaging," st 2000).
	Baird <i>et al.</i> , "Improved ΔΣ DAC Linearity Using Data Weighted Averaging", pp. 13-16 IEEE (1995).						, pp. 13-16,	
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	AR	<u>6</u>	Transactio	al., "A Low-Con ns on Circuits a January 1998)	nplexity Dynamic Element of Systems-II: Analog	ent Matching and Digital	g DAC for I Signal Pro	Direct Digital Sy cessing, Vol. 4	rnthesis," IEEE 5, No. 1, pp. 13-
	AS	<u>6</u>	Annovazzi Technolog	et al., "A Low-F y, "IEEE Journa	Power 98-dB Multibit Au al of Solid-State Circuits	udio DAC in s, Vol. 37, N	a Standard o. 7, pp. 82	d 3.3-V 0.35-µm 25-834, IEEE (J	n CMOS July 2002)
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	Fogleman et al., "A Digital Common-Mode Rejection Technique for Differential Analog-to- Digital Conversion," IEEE Transactions on Circuits and Systems-II: Analog and Digital Sign								
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